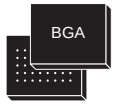
M68AW064F

1 Mbit (64K x16) 3.0V Asynchronous SRAM

FEATURES SUMMARY

- SUPPLY VOLTAGE: 2.7 to 3.6V
- 64K x 16 bits SRAM with OUTPUT ENABLE
- EQUAL CYCLE and ACCESS TIME: 55ns and 70ns
- LOW STANDBY CURRENT
- LOW V_{CC} DATA RETENTION: 2.0V
- TRI-STATE COMMON I/O
- AUTOMATIC POWER DOWN

Figure 1. Packages



TFBGA48 (ZB)
6 x 8 solder balls

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SUMMARY DESCRIPTION

The M68AW064F is a 1 Mbit (1,048,576 bit) CMOS SRAM, organized as 65,536 words by 16 bits. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single 2.7 to 3.6V supply. This device has an automatic power-down feature, reducing the power consumption by over 99% when deselected.

The M68AW064F is available in TFBGA48 (0.75 mm pitch) package.

Figure 2. Logic Diagram

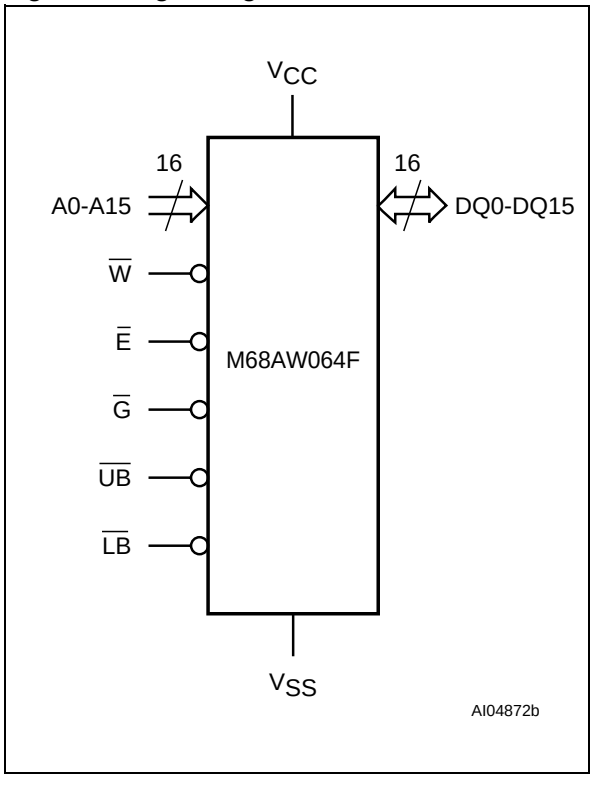


Table 1. Signal Names

A0-A15	Address Inputs
DQ0-DQ15	Data Input/Output
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{UB}$	Upper Byte Enable Input
$\overline{LB}$	Lower Byte Enable Input
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. TFBGA Connections (Top view through package)

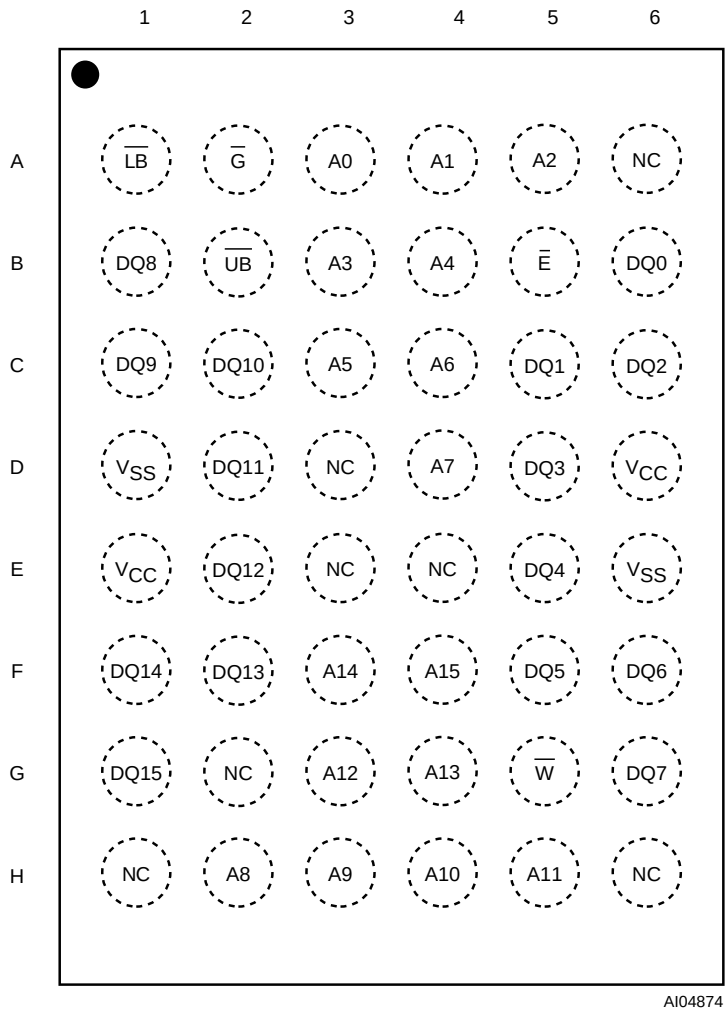
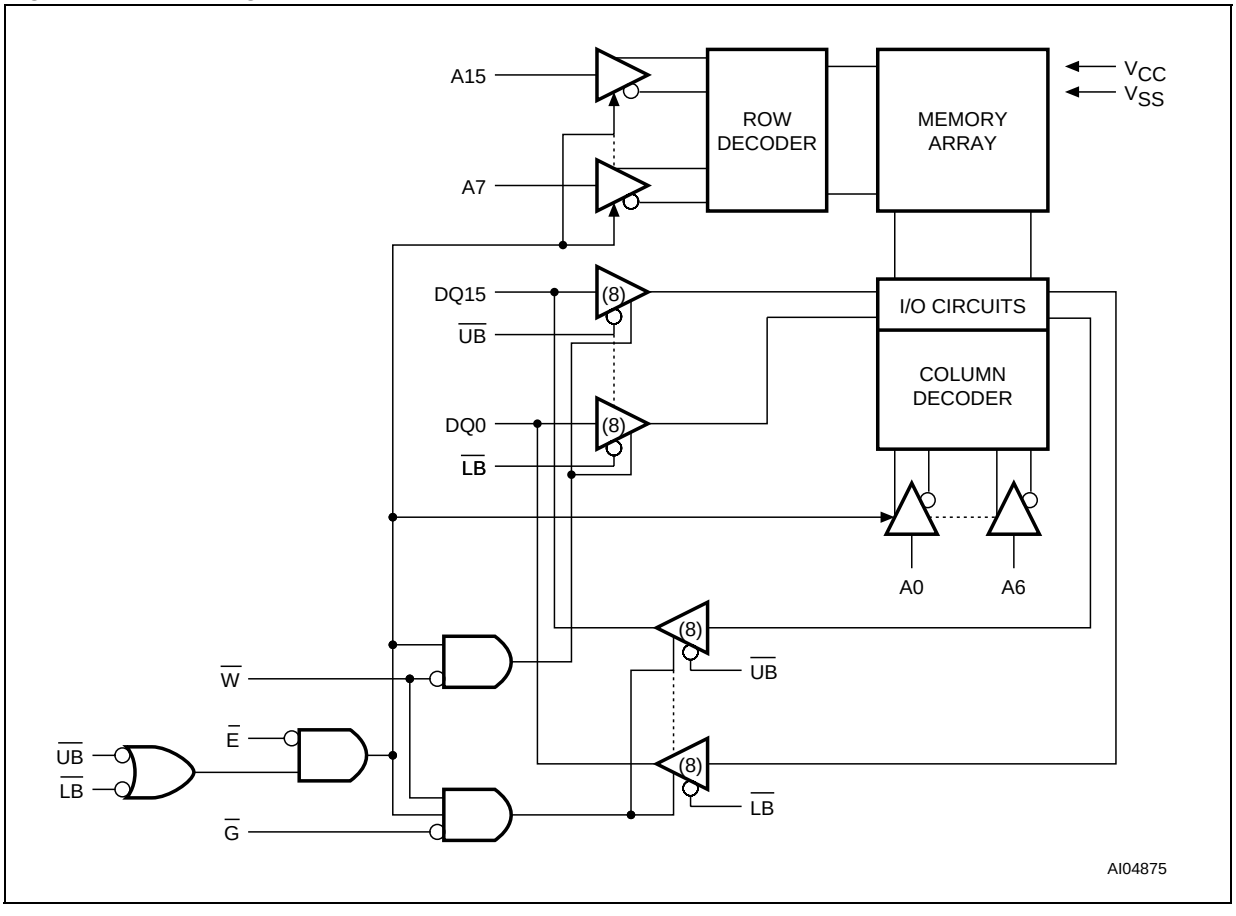


Figure 4. Block Diagram



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
I_O (1)	Output Current	20	mA
T_A	Ambient Operating Temperature	–55 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{CC}	Supply Voltage	–0.5 to 4.6	V
V_{IO} (2)	Input or Output Voltage	–0.5 to V_{CC} +0.5	V
P_D	Power Dissipation	1	W

Note: 1. One output at a time, not to exceed 1 second duration.
2. Up to a maximum operating V_{CC} of 3.6V only.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. Operating and AC Measurement Conditions

Parameter	M68AW064F
V_{CC} Supply Voltage	2.7 to 3.6V
Ambient Operating Temperature	–40 to 85°C
Load Capacitance (C_L)	30 or 5pF
Output Circuit Protection Resistance (R_1)	1.10kΩ
Load Resistance (R_2)	1.55kΩ
Input Rise and Fall Times	≤ 4ns
Input Pulse Voltages	0 to V_{CC}
Input and Output Timing Ref. Voltages	$V_{CC}/2$
Input and Output Transition Timing Ref. Voltages	$V_{OL} = 0.3V_{CC}$; $V_{OH} = 0.7V_{CC}$

Figure 5. AC Measurement I/O Waveform

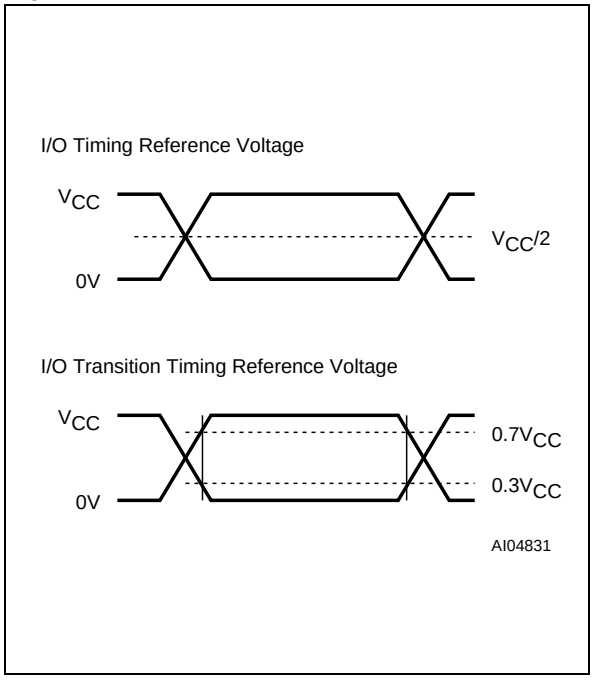


Figure 6. AC Measurement Load Circuit

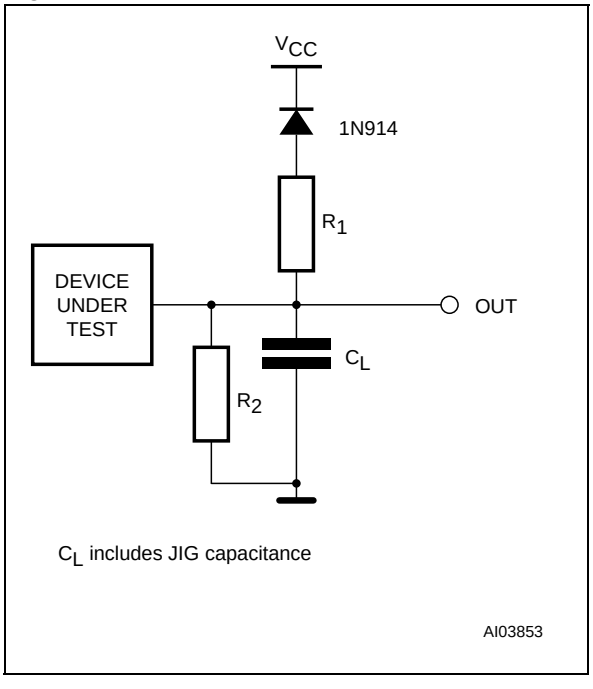


Table 4. Capacitance

Symbol	Parameter[1,2]	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		6	pF
C_{OUT}[3]	Output Capacitance	V_{OUT} = 0V		8	pF

Note: 1. Sampled only, not 100% tested.
2. At T_A = 25°C, f = 1 MHz, V_{CC} = 3.0V.
3. Outputs deselected.

Table 5. DC Characteristics

Symbol	Parameter	Test Condition	M68AW064F						Unit
			55			70			
			Min	Typ	Max	Min	Typ	Max	
I_{CC1} (1)	Operating Supply Current	V_{CC} = 3.6V, f = $1/t_{AVAV}$, I_{OUT} = 0mA		7	20			15	mA
I_{CC2}	Operating Supply Current	V_{CC} = 3.6V, f = 1MHz, I_{OUT} = 0mA		1	2		1	2	mA
I_{SB} (2)	Standby Supply Current CMOS	V_{CC} = 3.6V, $\overline{E} \geq V_{CC}$ –0.15V, f = 0		0.5	15		0.5	15	µA
I_{LI}	Input Leakage Current	$0V \leq V_{IN} \leq V_{CC}$	–1		1	–1		1	µA
I_{LO}	Output Leakage Current	$0V \leq V_{OUT} \leq V_{CC}$ (3)	–1		1	–1		1	µA
V_{IH}	Input High Voltage	V_{CC} = 2.7V	2.0		V_{CC} + 0.3	2.0		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	V_{CC} = 2.7V	–0.3		0.4	–0.3		0.4	V
V_{OH}	Output High Voltage	V_{CC} = 2.7V, I_{OH} = –1.0mA	2.2			2.2			V
V_{OL}	Output Low Voltage	V_{CC} = 2.7V, I_{OL} = 2.1mA			0.4			0.4	V

Note: 1. Average AC current, cycling at t_{AVAV} minimum.
2. All other Inputs at $V_{IL} \leq 0.15V$ or $V_{IH} \geq V_{CC}$ –0.15V.
3. Output disabled.

OPERATION

The M68AW064F has a Chip Enable power down feature which invokes an automatic standby mode whenever either Chip Enable is de-asserted ($\overline{E}$ = High) or $\overline{LB}$ and $\overline{UB}$ are de-asserted ($\overline{LB}$ and $\overline{UB}$ = High). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{E}$, $\overline{LB}$ and $\overline{UB}$ as summarized in the Operating Modes table (see Table 6).

Table 6. Operating Modes

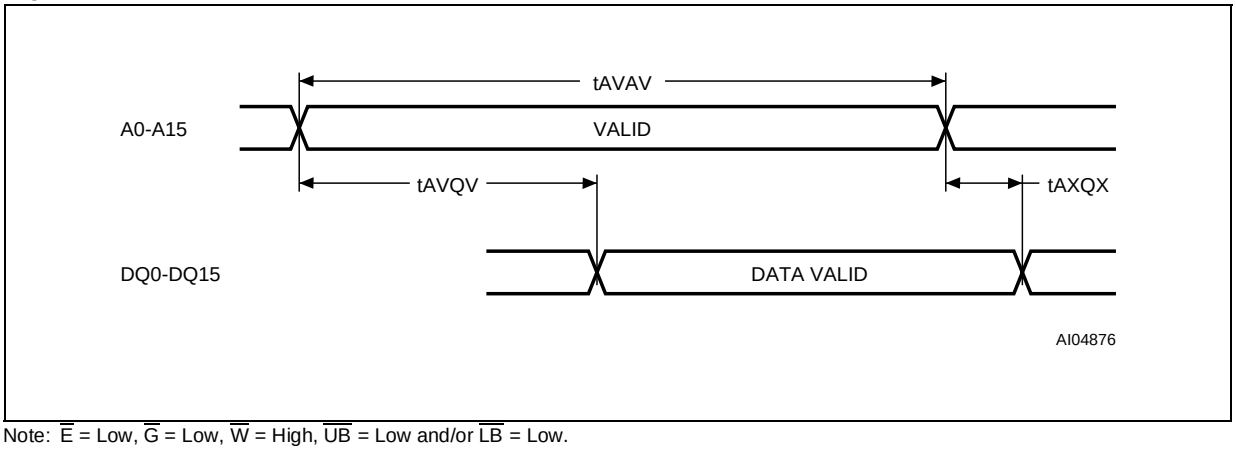
Operation	$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	DQ0-DQ7	DQ8-DQ15	Power
Deselected/Power-down	V_{IH}	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
Deselected/Power-down	X	X	X	V_{IH}	V_{IH}	Hi-Z	Hi-Z	Standby (I_{SB})
Lower Byte Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Output	Hi-Z	Active (I_{CC})
Lower Byte Write	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	Data Input	Hi-Z	Active (I_{CC})
Output Disabled	V_{IL}	X	V_{IH}	V_{IL}	X	Hi-Z	Hi-Z	Active (I_{CC})
Output Disabled	V_{IL}	X	V_{IH}	X	V_{IL}	Hi-Z	Hi-Z	Active (I_{CC})
Upper Byte Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Hi-Z	Data Output	Active (I_{CC})
Upper Byte Write	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	Hi-Z	Data Input	Active (I_{CC})
Word Read	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Data Output	Data Output	Active (I_{CC})
Word Write	V_{IL}	V_{IL}	X	V_{IL}	V_{IL}	Data Input	Data Input	Active (I_{CC})

Note: 1. X = V_{IH} or V_{IL}.

Read Mode

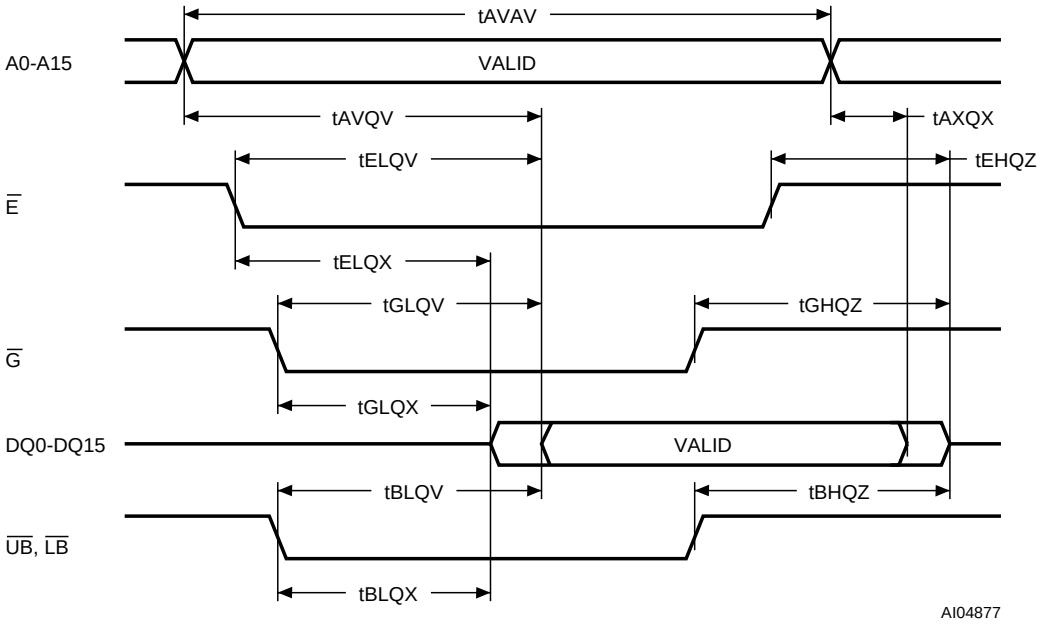
The M68AW064F is in the Read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and Chip Enable ($\overline{E}$) is asserted. This provides access to data from eight or sixteen, depending on the status of the signal $\overline{UB}$ and $\overline{LB}$, of the 1,048,576 locations in the static memory array, specified by the 16 address inputs. Valid data will be available at the eight or sixteen output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low and $\overline{E}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV}, t_{GLQV} or t_{BLQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, t_{GLQX} and t_{BLQX} but data lines will always be valid at t_{AVQV}.

Figure 7. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{W}$ = High, $\overline{UB}$ = Low and/or $\overline{LB}$ = Low.

Figure 8. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms.



Note: Write Enable ($\overline{W}$) = High.

Figure 9. Chip Enable or $\overline{UB}$/$\overline{LB}$ Controlled, Standby Mode AC Waveforms

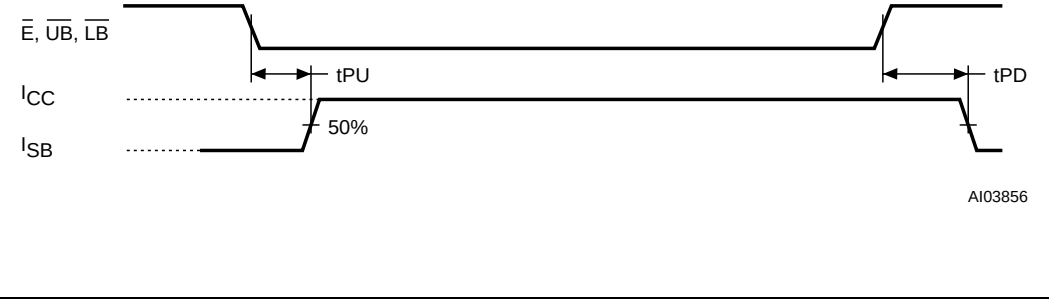


Table 7. Read and Standby Mode AC Characteristics

Symbol	Parameter	M68AW064F				Unit
		55		70		
		Min.	Max.	Min.	Max.	
t_{AVAV}	Read Cycle Time	55		70		ns
t_{AVQV}	Address Valid to Output Valid		55		70	ns
t_{AXQX}	Data hold from address change	10		10		ns
t_{BHQZ} (1, 2)	Upper/Lower Byte Enable High to Output Hi-Z		20		25	ns
t_{BLQV}	Upper/Lower Byte Enable Low to Output Valid		25		35	ns
t_{BLQX}	Upper/Lower Byte Enable Low to Output Transition	5		5		ns
t_{EHQZ} (1, 2)	Chip Enable High to Output Hi-Z		20		25	ns
t_{ELQV}	Chip Enable Low to Output Valid		55		70	ns
t_{ELQX}	Chip Enable Low to Output Transition	10		10		ns
t_{GHQZ} (1, 2)	Output Enable High to Output Hi-Z		20		25	ns
t_{GLQV}	Output Enable Low to Output Valid		25		35	ns
t_{GLQX}	Output Enable Low to Output Transition	5		5		ns
t_{PD}	Chip Enable or $\overline{UB}$/$\overline{LB}$ High to Power Down		55		70	ns
t_{PU}	Chip Enable or $\overline{UB}$/$\overline{LB}$ Low to Power Up	0		0		ns

Note: 1. At any given temperature and voltage condition, t_{GHQZ} is less than t_{GLQX}, t_{BHQZ} is less than t_{BLQX} and t_{EHQZ} is less than t_{ELQX} for any given device.
2. C_L = 5pF.

Write Mode

The M68AW064F is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ are Low. Either the Chip Enable input ($\overline{E}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. When $\overline{E}$ ($\overline{W}$) is Low, and $\overline{UB}$ or $\overline{LB}$ is Low, write cycle begins on the $\overline{W}$ ($\overline{E}$)'s falling edge. Therefore, address setup time is referenced to Write Enable as t_{AVWL} and to Chip Enable as t_{AVEL} and is determined by the latter occurring edge.

The Write cycle can be terminated by the earlier rising edge of $\overline{E}$ or $\overline{W}$.

If the Output is enabled ($\overline{E}$ = Low, $\overline{G}$ = Low, $\overline{LB}$ or $\overline{UB}$ = Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E}$, whichever occurs first, and remain valid for t_{WHDX} and t_{EHDX} respectively.

Figure 10. Write Enable Controlled, Write AC Waveforms

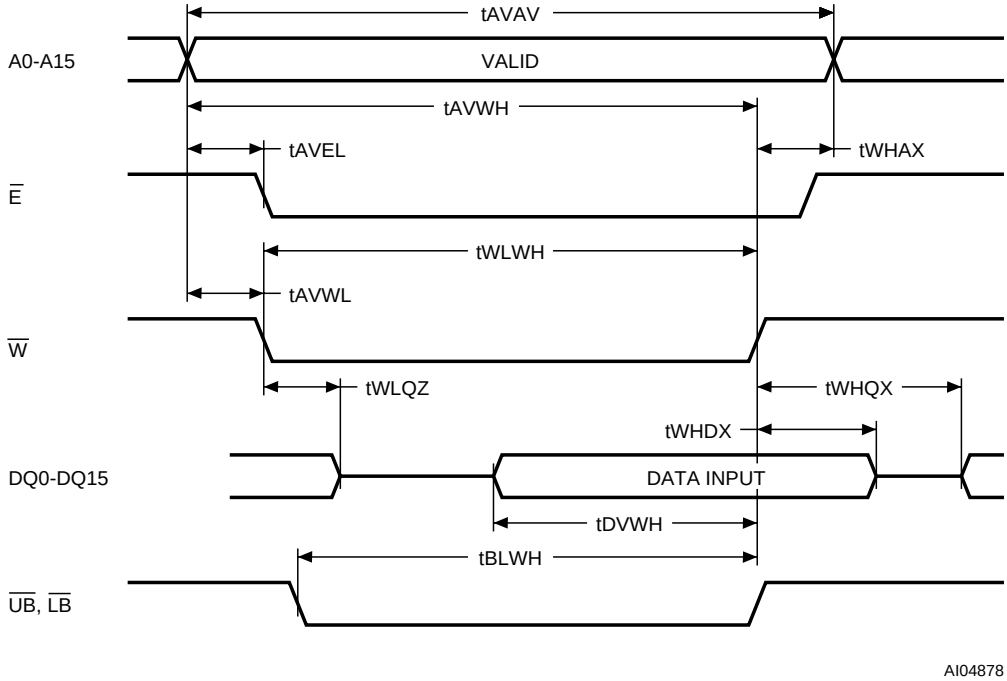


Figure 11. Chip Enable Controlled, Write AC Waveforms

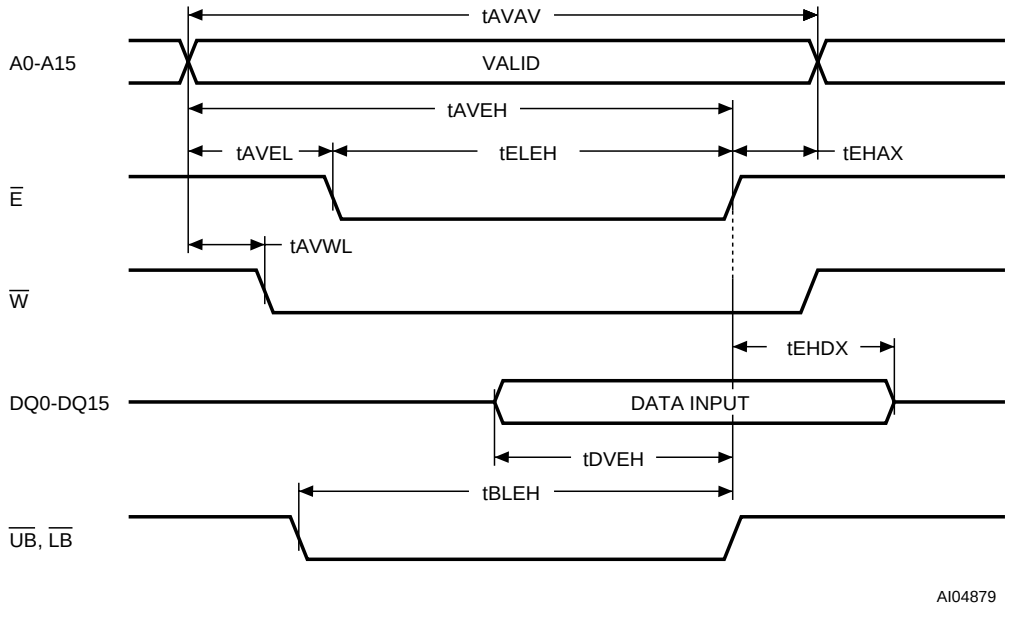


Table 8. Write Mode AC Characteristics

Symbol	Parameter	M68AW064F				Unit
		55		70		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	55		70		ns
t_{AVEH}	Address Valid to Chip Enable High	45		60		ns
t_{AVEL}	Address valid to Chip Enable Low	0		0		ns
t_{AVWH}	Address Valid to Write Enable High	45		60		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{BLEH}	$\overline{LB}$, $\overline{UB}$ Low to Chip Enable High	45		60		ns
t_{BLWH}	$\overline{LB}$, $\overline{UB}$ Low to Write Enable High	45		60		ns
t_{DVEH}	Input Valid to Chip Enable High	25		30		ns
t_{DVWH}	Input Valid to Write Enable High	25		30		ns
t_{EHAX}	Chip Enable High to Address Transition	0		0		ns
t_{EHDX}	Chip enable High to Input Transition	0		0		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	45		60		ns
t_{WHAX}	Write Enable High to Address Transition	0		0		ns
t_{WHDX}	Write Enable High to Input Transition	0		0		ns
t_{WHQX} (1)	Write Enable High to Output Transition	5		5		ns
t_{WLQZ} (1,2)	Write Enable Low to Output Hi-Z		25		25	ns
t_{WLWH}	Write Enable Low to Write Enable High	40		50		ns

Note: 1. At any given temperature and voltage condition, t_{WLQZ} is less than t_{WHQX} for any given device.
2. C_L = 5pF.

Figure 12. Low V_{CC} Data Retention AC Waveforms

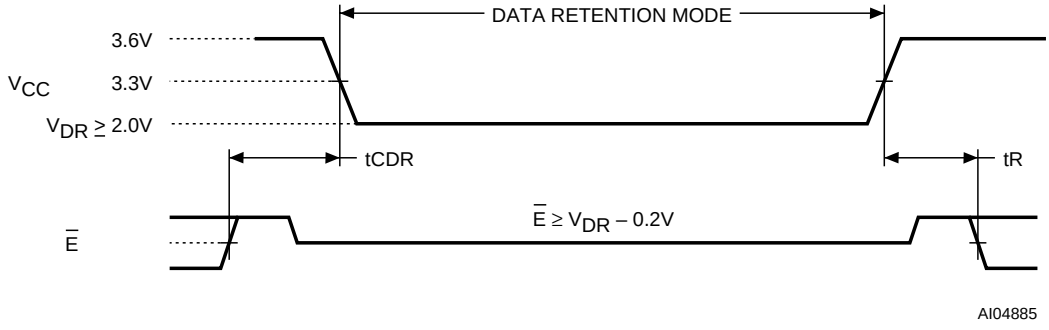


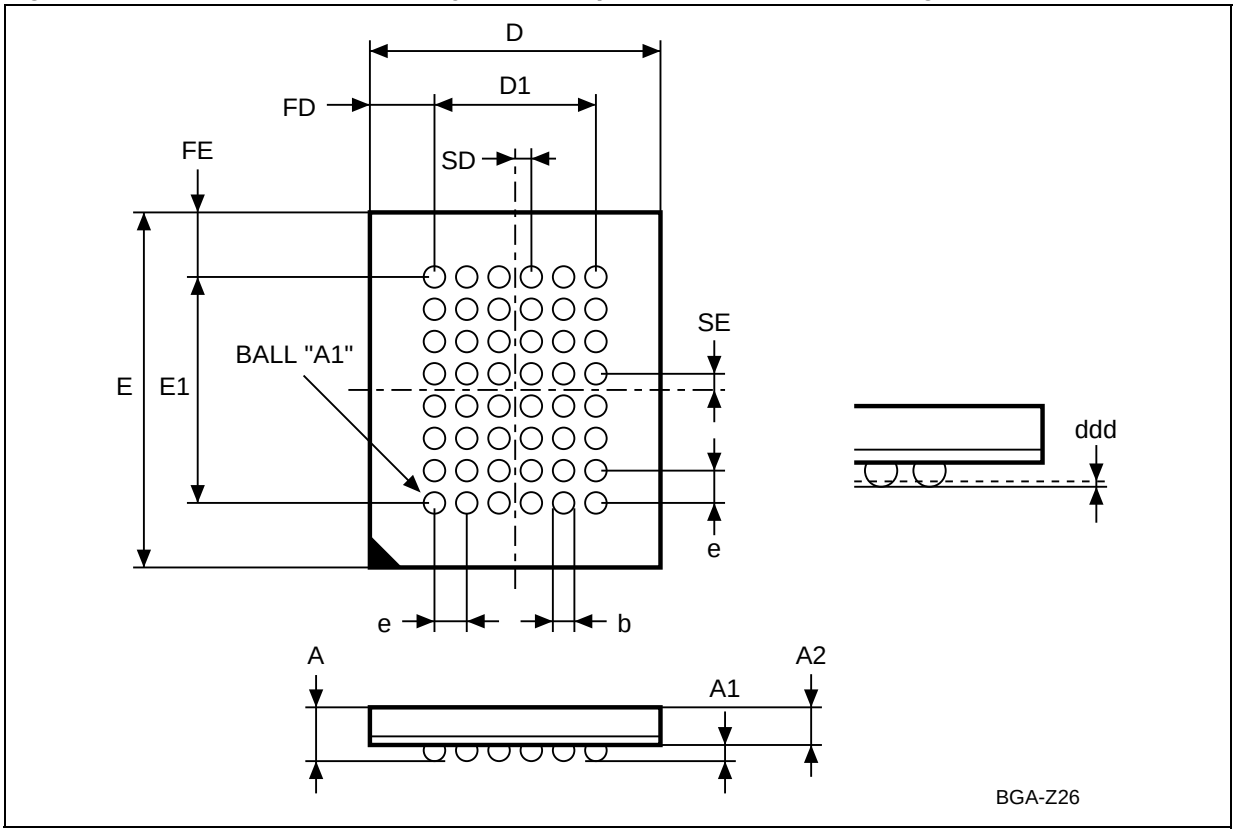
Table 9. Low V_{CC} Data Retention Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{CCDR} (1)	Supply Current (Data Retention)	V_{CC} = 2.0V, $\overline{E} \geq V_{CC}$ –0.3V, f = 0 (3)		0.5	15	µA
t_{CDR} (1,2)	Chip Deselected to Data Retention Time	$\overline{E} \geq V_{CC}$ –0.3V, f = 0	t_{AVAV}			ns
t_R (2)	Operation Recovery Time		0			ns
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E} \geq V_{CC}$ –0.3V, f = 0	2.0		3.6	V

Note: 1. All other Inputs at $V_{IH} \geq V_{CC}$ –0.2V or $V_{IL} \leq 0.2V$.
2. See Figure 12 for measurement points. Guaranteed but not tested. t_{AVAV} is Read cycle time.
3. No input may exceed V_{CC} +0.3V.

PACKAGE MECHANICAL

Figure 13. TFBGA48 - 6 x 8 ball array, 0.75 mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 10. TFBGA48 - 6 x 8 ball array, 0.75 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	6.000	5.900	6.100	0.2362	0.2323	0.2402
D1	3.750	–	–	0.1476	–	–
ddd			0.100			0.0039
E	8.000	7.900	8.100	0.3150	0.3110	0.3189
E1	5.250	–	–	0.2067	–	–
e	0.750	–	–	0.0295	–	–
FD	1.125	–	–	0.0443	–	–
FE	1.375	–	–	0.0541	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

PART NUMBERING

Table 11. Ordering Information Scheme

Example: M68AW064F L 55 ZB 6 T

Device Type
M68

Mode
A = Asynchronous

Operating Voltage
W = 2.7 to 3.6V

Array Organization
064 = 1 Mbit (64K x16)

Option 1
F = 1 Chip Enable; Standby from $\overline{UB}$ and $\overline{LB}$

Option 2
L = Low Leakage

Speed Class
55 = 55ns
70 = 70ns

Package
ZB = TFBGA48: 0.75 mm pitch

Operative Temperature
6 = –40 to 85 °C

Shipping
T = Tape & Reel Packing

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

REVISION HISTORY

Table 12. Document Revision History

Date	Version	Revision Details
July 2001	-01	First Issue
09-Oct-2002	1.1	Revision numbering modified: a minor revision will be indicated by incrementing the digit after the dot, and a major revision, by incrementing the digit before the dot (revision version 01 equals 1.0). Part number modified.
23-Apr-2003	1.2	55ns speed class added. Maximum Standby Supply Current I_{SB} modified. Values of certain AC Characteristics modified.